## LAB 09

## DECODER AND PRIORITY ENCODER

Decoder and Priority Encoder

Name: Muhammad Ahmed Baig

Roll: 20i-1884

Section: B

#### Objectives:

* + Practicing the implementation of logic functions using MSI level functional blocks
  + Gaining experience with MSI level functional blocks/components whose outputs are active low
  + Gaining a close insight into the functioning and properties of decoder circuits
  + Developing skills in the design and testing of combinational logic circuits.

#### Equipment Required:

* + DEV-2765E Trainer Board
  + 74LS138 (3-to-8 Decoder)
  + 74LS148 (8-bit Priority Binary Encoder)

#### Background Theory

Decoder is a multiple input, multiple output logic circuit that converts coded input into coded output, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is one-to-one mapping, each input code word produces a different output code word. The most commonly used input code is an n-bit binary code, where an n-bit word represents one of 2n different coded values, i.e n-to-2n decoder or binary decoder.

Encoder is a logic circuit that has fewer output bits than the input code. The encoder takes 2n inputs bits and generates n-bit output. Only one of the inputs can be 1, and the corresponding binary will display on the output bits. But when more than one input bits become 1 at the same time then what should be the output then? So we give priority to inputs and the input with high priority will freeze the output with its binary value. Such an encoder is called *priority encoder*.

### DECODER

#### Logic Diagram of 3-to-8 Decoder

D0



A2

A1

A0

D1

D2

D3

D4

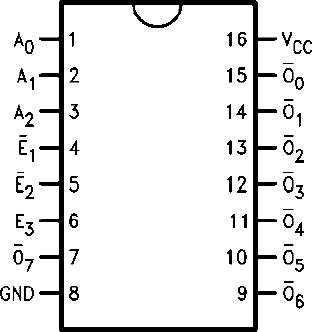
D5

D6

D7

Outputs are active low. The binary value on A2, A1, A0 will drive the corresponding output (Di) to 0 all other will remain at 1.

#### Pin Configuration of 74LS138 (3-to-8 Decoder)



**74LS138**

Proper value at the enable lines (E1=0, E2=0, E3=1) will enable the decoder, all other combination of enable lines will keep the output lines high. These multiple enable lines are for building large decoders.

### TRUTH TABLE

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **1** | **2** | **4** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| **E3** | **E2** | **E1** | **A0** | **A1** | **A2** | **O0** | **O1** | **O2** | **O3** | **O4** | **O5** | **O6** | **O7** |
| 1 | X | X | X | X | X | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| X | 1 | X | X | X | X | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| X | X | 0 | X | X | X | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| 0 | 0 | 1 | 0 | 0 | 0 | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| 0 | 0 | 1 | 1 | 0 | 0 | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** |
| 0 | 0 | 1 | 0 | 1 | 0 | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** |
| 0 | 0 | 1 | 1 | 1 | 0 | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **1** |
| 0 | 0 | 1 | 0 | 0 | 1 | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** |
| 0 | 0 | 1 | 1 | 0 | 1 | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |
| 0 | 0 | 1 | 0 | 1 | 1 | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** |
| 0 | 0 | 1 | 1 | 1 | 1 | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** |

#### Procedure

1. Connect the trainer with the power supply
2. Install the IC 74LS138 on the trainer board
3. IC 74138 is a 3 to 8 decoder / demultiplexer. Wire according to the diagram.
4. Use the logic switches for input and connect output O0 O1 ……O7 to the LEDs
5. Supply the VCC and GND to the pin 16 and 8 respectively
6. Test all the possible combination of input and fill out the table

### PRIORITY ENCODER (8-to-3)

I0

EO

I1 GS

I2

A0

I3

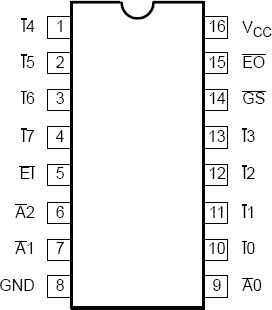
I4

A1

I5 I6

I7 A2

#### 74LS148 (8-to-3 Priority Encoder)



**74LS148**

EI=0 will drive the priority encoder, if EI=1 the output will all be 1’s as outputs are active low.

### TRUTH TABLE

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | | | | | | **OUTPUTS** | | | | |
| **EI** | **I0** | **I1** | **I2** | **I3** | **I4** | **I5** | **I6** | **I7** | **GS** | **A2** | **A1** | **A0** | **EO** |
| 1 | X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | X | X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | X | X | X | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

#### Procedue

1. Connect the trainer with the power supply
2. Install the IC 74LS148 on the trainer board
3. IC 74148 is 8 to 3 priority encoder. Wire according to the diagram.
4. Use the logic switches for input (I0,I1,…I7) and connect output (A2, A1, A0) to the LEDs.
5. Supply the VCC and GND to the pin 16 and 8 respectively
6. Test all the possible combination of input and fill out the table